**Low power area efficient ALU with low power full adder**

**Abstract**

This paper presents a low Power Area efficient ALU using XNOR logic. The 4bit ALU design is compared with various ALU implementation models with respect to their power consumption and area. ALU is an Arithmetic and Logic Unit, which performs arithmetic operation like ADD, SUB, PASS THROUGH, TWO'S COMPLEMENT, etc. and logic operation like AND, OR, EXCLUSIVE OR, EXCLUSIVE NOR, etc. We introduce a low power full adder, that consists of 8T which is generated using 3T XNOR logic and multiplexer. Full adder is the basic component for an ALU. By reducing the power of full adder, the ALU power also be reduced. Compared with Gate Diffusion Input Full Adder, 50% power reduced in the XNOR based Full Adder Technique. The simulation is carried out using cadence virtuoso 180nm technology, and compared with previous design of Gate Diffusion Input (GDI) technology. The result shows area efficient and low power consumption compared with Gate Diffusion Input technique.

**Tools:**

* Modelsim 6.4b
* Xilinx ISE 10.1

**Languages:**

* VHDL/Verilog HDL